

Mahesh R Panicker, PhD, Senior Member IEEE

CONTACT INFORMATION	Assistant Professor, Electrical Engineering, Indian Institute of Technology - Palakkad, Ahalia Integrated Campus, Kozhippara, Palakkad, Kerala 678557 India	<i>Phone:</i> (+91) 49 2322 6422 <i>E-mail:</i> mahesh@iitpkd.ac.in <i>WWW:</i> https://iitpkd.ac.in/people/mahesh
RESEARCH INTERESTS	Reconfigurable Digital Signal Processing, Low Power / Area Efficient Circuits and Systems, Diagnostic Ultrasound Imaging, Biomedical Circuits and Systems	
EDUCATION	Doctor of Philosophy (PhD) School of Computer Engineering, Nanyang Technological University (NTU), Singapore <ul style="list-style-type: none">• Dissertation Topic: “Reconfigurable low complexity digital filter banks for software radio receivers”• Advisor: Assoc. Prof. A. P. Vinod (NTU, Singapore)	<i>July 2005 - July 2008</i>
	Bachelor of Technology (B.Tech (Hons)) Department of Electrical and Electronics Engineering, Rajiv Gandhi Institute of Technology (Govt. Engineering College), Mahatma Gandhi University, Kerala, India <ul style="list-style-type: none">• Percentage Marks: 88% (First Rank in the University)• FYP Title: “Microprocessor based Autonomous Robot”• Advisor: Dr. Dinesh Gopinath , Asst.Professor in Electrical Engineering, College of Engineering, Thiruvananthapuram, Kerala, India.	<i>Nov 1999 - July 2003</i>
EMPLOYMENT HISTORY	Indian Institute of Technology, Palakkad <i>Assistant Professor</i> in Electrical Engineering, Indian Institute of Technology, Palakkad. Involved in research and development of advanced signal processing, analytics and imaging techniques for diagnostic ultrasound systems.	<i>June 2018 - Till Now</i>
	Samsung Research, Bangalore <i>Senior Chief Engineer</i> at Ultrasound Systems, Healthcare and Medical Equipments (HME), Samsung Research Institute, Bangalore, India. Involved in research, development and productization of advanced signal processing, analytics and imaging techniques for diagnostic ultrasound systems.	<i>May 2017 - May 2018</i>
	General Electric (GE) Global Research, Bangalore <i>Lead Engineer</i> at Software Sciences and Analytics Research, GE Global Research, John F Welch Technology Center, Bangalore, India. Helped in establishing diagnostic ultrasound imaging lab in GE Global Research, Bangalore and in establishing collaboration with General Imaging business, GE Healthcare, Milwaukee. Involved in development of advanced analytics, signal processing algorithms/systems for applications in health care, energy, oil and gas and transportation domains. Filed 10 patents and involved in many of the popular GE products such as diagnostic ultrasound systems, non-invasive neonatal/fetal heart rate monitoring, compressor blade health monitoring (BHM) and Tier4 locomotive prognostics.	<i>Aug 2010 - April 2017</i>
	Nanyang Technological University (NTU), Singapore <i>Research Fellow</i> at Center for High Performance Embedded Systems (ChiPES), NTU, Singapore. Involved in development of novel reconfigurable low complexity spectrum sensing algorithms and architectures for military and cognitive radios.	<i>Aug 2008 - July 2010</i>

SUPELEC, Rennes, France*Nov 2007 - Dec 2007*

Sponsored Internship at SUPELEC in the Signal, Communication et Electronique Embarquee (SCEE) team as part of Merlion Project Grant (Dossier No. 9.03.07), France-Singapore Cooperation Platform in Science and Technology.

Involved in development of novel spectrum sensing architectures for cognitive radio.

Nanyang Technological University (NTU), Singapore*Aug 2008 - July 2010*

Teaching Assistance at School of Computer Engineering, NTU, Singapore.

Handled sessions in Instrumentation and Data Acquisition Lab and Digital Systems Lab.

Mahatma Gandhi University, Kottayam, Kerala , India*Aug 2003 - July 2005*

Lecturer at SAINTGITS College of Engineering, MG University, Kerala, India.

Taught basic and advanced courses in Electrical and Electronics Engineering.

HONORS

- Nanyang PhD Scholarship, NTU Singapore.
- Gold medal for topper in B.Tech (EEE), Mahatma Gandhi University, Kerala, India
- 2015 GE Global Research Annual Award for Exemplifying GE Purpose and Innovation
- 2013 GE Technical Excellence Award in Services Technologies
- 2013 GE Customer Site Demonstration Award for Tier4 Locomotive Analytics
- 2012 GE Customer Site Demonstration Award for Compressor Blade Health Monitoring
- 11 GE Technical Expertise Awards - 2011 - 2017

**PROFESSIONAL
ACTIVITIES**

- Senior Member, IEEE
- MATRIZ TRIZ Level 2 Certification (TRIZ Practitioner)
- Member, Technical Committee on Brain-Machine Interface Systems, IEEE Systems, Man and Cybernetics Society
- Member, IEEE Signal Processing Society
- Member, IEEE Communications Society
- Member, IEEE Systems, Man and Cybernetics Society
- Six Sigma Green Belt Certification
- Session Chair, Biomedical Systems, IEEE Region-10 Conference, TENCON 2020
- Program Committee, International Symposium on Electronic System Design (ISED), 2011-2014
- Program Committee, International Conference on Eco-friendly Computing and Communication Systems (ICECCS 2013)
- Program Committee, International Conference on Advances in Computing and Communications (ACC 2013)
- Track Chair, IEEE International Conference on Information, Communications and Signal Processing (ICICS 2009).
- Reviewer of IEEE Transactions on Signal Processing, IEEE Transactions on Circuits and Systems - I and II, IEEE Transactions on Vehicular Technology, IEEE Transactions on VLSI Systems, IET Transactions on Signal Processing, Springer Journal of Signal Processing Systems for Signal, Image and Video Technology and International conferences such as ISCAS, ICCS, ICICS, TENCON, SPCOM

RESEARCH GRANTS

Title: Development of a Real Time Spectral Analysis and Filtering System Based on Lyrtech SFF

Role: Co-Investigator with Assoc. Prof. Vinod A Prasad, NTU.

Funding Organization: Temasek Laboratories/DSO National Labs, Defence Science and Technology Agency (DSTA), Singapore

Amount: 64000 SGD

Duration: September 2008 - September 2009

Title: Investigation of a portable, affordable and self-guided bedside ultrasound system for tissue and blood velocity imaging

Role: Principal Investigator

Funding Organization: Early Career Research (ECR) award, Science and Engineering Research Board (SERB), India

Amount: Rs 49,01,830

Duration: March 2019 - March 2022

Title: Assistive and Rehabilitation Technology Development

Role: Co-Principal Investigator

Funding Organization: GadgEon Smart Systems, Kochi, India

Amount: Rs 17,30,000

Duration: 2 years (Not Started)

PUBLICATIONS:
PATENTS

1. Method of inspection for corrosion under insulation - Part I- System (Filed Jul 2011).
2. Method of inspection for corrosion under insulation - Part II- Algorithms (Filed Jul 2011).
3. Methods and system to monitor health of rotor blades - Part I (<http://patents.justia.com/patent/20150184536>).
4. Methods and system to monitor health of rotor blades - Part II (<http://patents.justia.com/patent/20160169765>).
5. Methods and systems to determine rotor imbalance - Part I (Filed Dec 2013).
6. Methods and systems to determine rotor imbalance - Part II (<http://patents.justia.com/patent/20160169765>).
7. System and method for monitoring machines (<http://patents.justia.com/patent/20150369687>).
8. Systems and methods for inspecting reinforced concrete structures (<https://www.google.com/patents/US20150115980>)
9. Method and system for measuring a volume of an organ of interest (<https://patents.google.com/patent/US20180085043A1>)
10. System and method for imaging deeper tissues (Filed Feb 2017)

PUBLICATIONS:
PUBLISHED
JOURNALS

10. Gayathri M and **Mahesh Raveendranatha Panicker**, "Towards A Pixel-Level Reconfigurable Digital Beamforming Core for Diagnostic Ultrasound Imaging," accepted for publication in *IEEE Transactions on Biomedical Circuits and Systems*, March 2020
9. **R. Mahesh** and A. P. Vinod, "An area-efficient non-uniform filter bank for low overhead reconfiguration of multi-standard software radio channelizers," *Journal of Signal Processing Systems for Signal, Image and Video Technology* (formerly the Journal of VLSI Signal Processing Systems for Signal, Image and Video Technology), Springer, vol. 64, no. 3, pp.413-428, Sep. 2011.
8. **R. Mahesh** and A. P. Vinod, "A low complexity flexible spectrum sensing scheme for mobile cognitive radio terminals," *IEEE Transactions on Circuits and Systems II*, vol. 58, no. 6, pp.371-375, June 2011.
7. **R. Mahesh** and A. P. Vinod, "Low complexity flexible filter banks for uniform and non-uniform channelization in software radios using coefficient decimation," *IET Circuits, Devices and Systems*, vol. 5, no. 3, pp.232-242, May 2011.
6. **R. Mahesh** and A. P. Vinod, "A Reconfigurable Low Area Complexity Filter Bank Architec-

ture based on Frequency Response Masking for Non-Uniform Channelization in Software Radio Receivers,” *IEEE Transactions on Aerospace and Electronic Systems*, pp. 1241-1255, vol. 47, no. 2, April 2011.

5. **R. Mahesh** and A. P. Vinod, “New reconfigurable architectures for implementing FIR filters with low complexity,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 2, pp.275-288, Feb. 2010.
4. **R. Mahesh**, A. P. Vinod, E. M-K. Lai and Amos Omondi, “Filter bank channelizers for multi-standard software defined radio receivers,” *Journal of Signal Processing Systems for Signal, Image and Video Technology*, Springer, Article in Press: DOI 10.1007/s11265-008-0327-y.
3. Jimson Mathew, **R. Mahesh**, A. P. Vinod and Edmund M-K. Lai, “Realization of low power high-speed channel filters with stringent adjacent channel attenuation specifications for wireless communication receivers,” *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E91-A, no.9, pp. 2564-2570, September 2008.
2. **R. Mahesh** and A. P. Vinod, “Reconfigurable frequency response masking filters for software radio channelization,” *IEEE Transactions on Circuits and Systems-II*, pp.274-278, vol. 55, no. 3, March 2008.
1. **R. Mahesh** and A. P. Vinod, “A new common subexpression elimination algorithm for realizing low complexity higher order digital filters,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 217-229, vol. 27, no. 2, Feb. 2008.

PUBLICATIONS:
CONFERENCES

28. Gayathri M and **Mahesh Raveendranatha Panicker**, ”VLSI architectures for Delay Multiply and Sum Beamforming in Ultrasound Medical Imaging,” in Proc. of IEEE SPCOM 2020, Bangalore, July 2020.
27. Madhavanunni A.N. and **Mahesh Raveendranatha Panicker**, ” Directional beam focusing based dual apodization approach for improved vector flow imaging ”, in Proc. of IEEE ISBI 2020, Iowa City, April 2020.
26. Madhavanunni A.N. and **Mahesh Raveendranatha Panicker**, ”Triangulation based vector flow imaging with non-steered plane waves for transverse flows”, in Proc. of SPIE Medical Imaging 2020, Houston, Feb 2020. (Shortlisted for Robert F Wagner Best Student Paper Award)
25. Samhitha Rachakonda and **R. Mahesh** ”Automated Noise Detection and Classification for Unsupervised ECG Analysis Systems Using CEEMD and Wavelet Packet Decomposition ,” in Proc. of TENCON 2019, Kochi, India, September 2019.
24. **R. Mahesh**, P. Bhushan, Ek Tsoon Tan, J. Suresh, M. Radhika, M. Luca, M. Rakesh, Improving neighborhood voxel correlation in resting state fMRI using BOLD signal decomposition ,” in Proc. of OHBM 2016, Geneva, Switzerland, June 2016.
23. P. Bhushan, **R. Mahesh**, Ek Tsoon Tan, J. Suresh, M. Radhika, M. Luca, M. Rakesh, Spatiotemporal denoising in resting state fMRI,” in Proc. of OHBM 2016, Geneva, Switzerland, June 2016.
22. P. Bhushan, **R. Mahesh**, M. Radhika, J. Suresh, Group NMF analysis for resting state fMRI,” in Proc. of ISMRM 2016, Singapore, May 2016.
21. **R. Mahesh**, P. Bhushan, Ek Tsoon Tan, J. Suresh, Blind functional clustering of resting state fMRI using non-negative matrix factorization,” in Proc. of OHBM 2016, Hawaii, June 2015.
20. P. Bhushan, **R. Mahesh**, Ek Tsoon Tan, J. Suresh, Optimal wavelet basis selection for resting state fMRI analysis,” in Proc. of OHBM 2016, Hawaii, June 2015.
19. Smitha K. G., A. P. Vinod and **R. Mahesh**, “Reconfigurable area and power efficient I-Q mapper for adaptive modulation,” in Proc. of *54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Seoul, South Korea, August 2011.
18. Smitha K. G., **R. Mahesh** and A. P. Vinod, “Challenges in digital filter bank implementation from a cognitive radio perspective - A review,” in Proc. of *Asia-Pacific Signal and Information Processing Association (APSIPA) Annual Summit and Conference*, Singapore, December 2010.
17. **R. Mahesh** and A. P. Vinod, “Reconfigurable discrete Fourier transform filter banks for variable resolution spectrum sensing,” in Proc. of *IEEE International Conference on Communication Systems*, November 2010, Singapore.
16. **R. Mahesh** and A. P. Vinod, “Reconfigurable discrete Fourier transform filter banks for multi-

- standard channelizers,” in Proc. of *IEEE International Conference on Signal Processing and Communications*, Bangalore, India, July 2010. (SPCOM 2010).
15. S. J. Darak, A. P. Vinod, **R. Mahesh** and E. M-K. Lai “A reconfigurable filter bank for uniform and non-uniform channelization in multi-standard wireless communication receivers,” in Proc. of the *17th IEEE International Conference on Telecommunications*, Doha, Qatar, April 2010. (ICT 2010).
 14. **R. Mahesh**, A. P. Vinod, B. Y. Tan and E. M-K. Lai, “A tree-structured non-uniform filter bank for multistandard wireless receivers,” in Proc. of *IEEE International Symposium on Circuits and Systems*, Taiwan, May 2009. (ISCAS 2009).
 13. S. T. Gul, **R. Mahesh**, C. Moy, A. P. Vinod and Jacques Palicot, “A graphical approach for the optimization of SDR channelizers,” in Proc. of *URSI (International Union of Radio Science) General Assembly*, Chicago, USA, August 2008.
 12. **R. Mahesh** and A. P. Vinod, “Reconfigurable filter banks for software defined radio receivers – An alternative low complexity design to conventional DFT filter banks,” in Proc. of *URSI (International Union of Radio Science) General Assembly*, Chicago, USA, August 2008.
 11. **R. Mahesh**, A. P. Vinod, Christophe Moy and Jacques Palicot, “A low complexity reconfigurable filter bank architecture for spectrum sensing in cognitive radios,” in Proc. of *3rd International Conference on Cognitive Radio Oriented Wireless Networks and Communications*, Singapore May 2008. (CROWNCOM 2008).
 10. Smitha K. G., **R. Mahesh** and A. P. Vinod, “A reconfigurable multi-stage frequency response masking filter bank architecture for software defined radio receivers,” in Proc. of *IEEE International Symposium on Circuits and Systems*, Seattle, USA, May 2008. (ISCAS 2008).
 9. **R. Mahesh** and A. P. Vinod, “Coefficient decimation approach for realizing reconfigurable finite impulse response filters,” in Proc. of *IEEE International Symposium on Circuits and Systems*, Seattle, USA, May 2008. (ISCAS 2008).
 8. Jimson Mathew, **R. Mahesh**, A. P. Vinod and E. M-K. Lai, “Realization of low power high-speed channel filters with stringent adjacent channel attenuation specifications for software radio receivers,” in Proc. of *Sixth IEEE International Conference on Information, Communications and Signal Processing*, Singapore, December 2007. (ICICS 2007).
 7. **R. Mahesh** and A. P. Vinod, “A new low complexity reconfigurable filter bank architecture for software radio receivers based on interpolation and masking technique,” in Proc. of *Sixth IEEE International Conference on Information, Communications and Signal Processing*, Singapore, December 2007. (ICICS 2007).
 6. G. Deepak, **R. Mahesh** and A. Sluzek, “Adaptable area-efficient parallel architecture for grey and color image convolvers,” in Proc. of *IEEE International Symposium on Signals, Circuits and Systems*, 2007, pp. 1-4, Vol. 2, July 2007. (ISSCS 2007).
 5. **R. Mahesh** and A. P. Vinod, “An architecture for integrating low complexity and reconfigurability for channel filters in software defined radio receivers,” in Proc. of *IEEE International Symposium on Circuits and Systems*, pp. 2514- 2517, May 2007, USA. (ISCAS 2007).
 4. **R. Mahesh** and A. P. Vinod, “Frequency response masking based reconfigurable channel filters for software radio receivers,” in Proc. of *IEEE International Symposium on Circuits and Systems*, pp. 2518-2521, May 2007, USA. (ISCAS 2007).
 3. G. Deepak, **R. Mahesh** and A. Sluzek, “Design of an area-efficient multiplierless processing element for fast two dimensional image convolution,” in Proc. of *13th IEEE International Conference on Electronics, Circuits and Systems*, pp.467-470, Dec. 2006 (ICECS 2006).
 2. **R. Mahesh** and A. P. Vinod, “Reconfigurable low complexity FIR filters for software radio receivers,” in Proc of *17th IEEE International Symposium on Personal, Indoor and Mobile radio communications*, pp. 1-5, Finland, Sep. 2006. (PIMRC 2006).
 1. **R. Mahesh** and A. P. Vinod, “A new common subexpression elimination algorithm for implementing low complexity FIR filters in software defined radio receivers,” in Proc. of *IEEE International Symposium on Circuits and Systems*, pp. 4515 – 4518, Greece, May 2006. (ISCAS 2006).

plementation of Signal Processing Algorithms on DSP Processors", PSG Coimbatore, 16th December 2019

"From the physical world to the digital world: enabling machine learning driven by domain knowledge" *IEEE SPS Kerala Section - Colloquium on ML with Signal Processing for Data Analytics*", CUSAT, Kochi, 28th September 2019

"Signal Processing In The Era of Big Data" *National Conference on Communication, Computing and System Design (NC³SSD'19)* , PSGiTech, Coimbatore, 19th March 2019

"Compressive Sampling - A Paradigm Shift in Digital Signal Processing", *Workshop on Advances in Signal and Image Processing*, GITAM University, Vishakapatnam, Feb 2014

"Advances in Industrial Digital Signal Processing", *Technical Quality Improvement Program (TQIP) for Faculty on Advances in Digital Systems*, Cochin University of Science and Technology (CUSAT), Kochi, June 2011

"Reconfigurable Low Complexity Digital Filters", *Military Radio Lecture Series*, NTU, Singapore, Feb 2009

"Reconfigurable Low Complexity Spectrum Sensing", *Visitor Lecture Series*, SUPELEC, Rennes, France, Dec 2008

"Reconfigurable Low Complexity Digital Filter Banks for Software Radio Receivers", *Graduate Students Workshop organized by IEEE CAS society*, Singapore, September 2007.